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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,893	09/30/2003	John A. Rushing	42P14977	8058

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INTEL CORPORATION
c/o INTELLEVATE, LLC
P.O. BOX 52050
MINNEAPOLIS, MN 55402

EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,893	RUSHING ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/676893, file on 09/30/03.

Claim 1-26 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Ku et al. (US Patent 6792585).

3. As to claim 1, Ku et al. teach a method comprising: representing each vector associated with an integrated circuit datapath design as one of a row and a column (see fig 2a, 2b and summary); and representing each bit slice associated with the integrated circuit datapath design in an orthogonal manner to the vectors, the corresponding vector and bit slice representation being different than an associated physical layout (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

4. As to claim 2, Ku et al. teach further comprising: using similar visual representations to indicate cell similarities (see fig 4a col 3 line 60 to col 4 line 63).

5. As to claim 3, Ku et al. teach wherein representing each vector includes representing each vector as a row, and wherein representing each bit slice includes representing each bit slice as a column (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

6. As to claim 4, Ku et al. teach further comprising: representing information indicating connectivity between a selected vector and at least one of another vector and interface pins (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

7. As to claim 5, Ku et al. teach further comprising providing drag and drop editing capabilities to move a vector (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

8. As to claim 6, Ku et al. teach wherein, each vector includes a plurality of cell instances, and wherein, providing drag and drop editing capabilities includes providing drag and drop editing capabilities to move a group of cell instances (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

9. As to claim 7, Ku et al. teach An apparatus comprising: a vector extraction engine to extract vectors from an input file associated with an integrated circuit design (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17); and a vector editor to provide a graphical interface to represent and edit the extracted vectors as one of a row and a column and to represent bit slices in an orthogonal manner to the extracted vectors (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

10. As to claim 8, Ku et al. teach wherein the graphical interface is further to represent similar cells associated with the integrated circuit design using a similar visual representation (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

11. As to claim 9, Ku et al. teach wherein the vector extraction engine is to extract vectors using a name-based vector extraction approach (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

12. As to claim 10, Ku et al. teach wherein the vector extraction engine is to extract vectors using a bus/connectivity- based vector extraction approach (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background).

13. As to claim 11, Ku et al. teach wherein the graphical interface is further to represent similar cells associated with the integrated circuit design using a similar color and stippling (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and summary).

14. As to claim 12, Ku et al. teach wherein the vector editor is further to assign one of a plurality of predetermined visual representations to each cell type associated with the integrated circuit design (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

15. As to claim 13, Ku et al. teach wherein the vector editor is further to visually represent connectivity information indicating connections between a vector and one of another vector and an interface pin (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

16. As to claim 14, Ku et al. teach wherein the graphical interface is further to provide drag and drop editing capabilities to move one or more of vectors, bit slices, and connections (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and abstraction).

17. As to claim 15, Ku et al. teach wherein the vector editor is to provide data to a placement engine, the placement engine to output a datapath placement associated with the integrated circuit design (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background).

18. As to claim 16, Ku et al. teach wherein the vector editor is further to provide at least one metric indicating a quality of the data provided by the vector editor (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

19. As to claim 17, Ku et al. teach wherein the vector editor provides at least one of an auto-merge and an auto-align command (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17).

20. As to claim 18, Ku et al. teach a computer-accessible storage medium storing information that, when accessed by a machine, causes the machine to: represent vectors associated with an integrated circuit datapath design in one of a row and a column (see fig 2a, 2b and summary); and represent bit slices associated with the integrated circuit datapath design in an orthogonal manner, wherein the manner in which the vectors and bit slices is represented is different than an associated physical layout (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

21. As to claim 19, Ku et al. teach further storing information that, when accessed by a machine, causes the machine to: represent connectivity between a vector and one of another vector and an interface pin (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 3 line 59).

22. As to claim 20, Ku et al. teach further storing information that, when accessed by a machine, causes the machine to: extract the vectors from an input file associated with the integrated circuit datapath design (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background).

23. As to claim 21, Ku et al. teach wherein extracting the vectors from the input file includes using a name-based extraction approach (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background).

24. As to claim 22, Ku et al. teach wherein extracting the vectors from the input file includes using a bus/connectivity- based extraction approach (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background).

25. As to claim 23, Ku et al. teach an apparatus comprising: a vector editor to represent vectors associated with an integrated circuit datapath design as one of rows and columns and bit slices associated with the integrated circuit datapath design in an orthogonal manner, wherein the row and column representation is different than an associated physical layout, the vector editor to provide one of an auto-merge and an auto-align command to operate on the vectors (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background); and a placement engine to receive an output of the vector editor and to produce an associated placement (see fig 2a, fig 2b, and fig 3 col 2 line 60 to col 5 line 17 and background).

26. As to claim 24, Ku et al. teach wherein, the vector editor is further to use similar visual representations to identify similar cell instances (see fig 4a fig 4b col 3 line 60 to col 5 line 6).

27. As to claim 25, Ku et al. teach wherein, similar visual representations includes a combination of a similar color and a similar stippling technique (see fig 4a fig 4b col 3 line 60 to col 5 line 6 and background).

28. As to claim 26, Ku et al. teach wherein, the vector editor provides drag and drop editing capabilities to edit the vectors, bit slices and associated connectivity (see fig 4a fig 4b col 3 line 60 to col 5 line 6 and summary).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Binh Tat
Art unit 2825
March 2, 2005

THUAN DO
Primary examiner
3/18/06